**实验报告**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 姓名 | 徐时越 | 学号 | 16058228 | 班级 | 16059611 |
| 专业 | 软件工程 | | 课程名称 | 计算机组成原理课程设计 | |
| 任课老师 | 仇建 | 指导老师 | 仇建 | 机位号 |  |
| 实验序号 | 5 | 实验名称 | 存储器设计实验 | | |
| 实验时间 |  | 实验地点 |  | 实验设备号 |  |
| **一、实验程序源代码** | | | | | |
| 程序源代码  module RAM\_A(Mem\_Addr,Switch,Mem\_Write,Clk,LED);  input wire [7:2]Mem\_Addr;  input wire [1:0] Switch;  input wire Mem\_Write;  input wire Clk;  output reg [7:0] LED;  reg [31:0] REG\_Files[0:63];  reg [6:0] i;  reg [31:0] M\_R\_Data;  reg [31:0] M\_W\_Data;  initial  begin  for(i=0;i<=63;i=i+1)  REG\_Files[i]=0;  end  always@(posedge Clk)  begin  if(Mem\_Write)  REG\_Files[Mem\_Addr]=M\_W\_Data;  end  always@(Mem\_Addr,Mem\_Write,Switch)  begin  if(!Mem\_Write)  begin  M\_R\_Data=REG\_Files[Mem\_Addr];  case(Switch)  2'b00:LED=M\_R\_Data[7:0];  2'b01:LED=M\_R\_Data[15:8];  2'b10:LED=M\_R\_Data[23:16];  2'b11:LED=M\_R\_Data[31:24];  endcase  end  else  begin  case(Switch)  2'b00:M\_W\_Data=32'h0000\_0001;  2'b01:M\_W\_Data=32'h0001\_0000;  2'b10:M\_W\_Data=32'h1F1F\_F1F1;  2'b11:M\_W\_Data=32'hFFFF\_FFFF;  endcase  end  end  endmodule  仿真代码  module Test\_RAM\_A;  // Inputs  reg [7:2] Mem\_Addr;  reg [1:0] Switch;  reg Mem\_Write;  reg Clk;  // Outputs  wire [7:0] LED;  // Instantiate the Unit Under Test (UUT)  RAM\_A uut (  .Mem\_Addr(Mem\_Addr),  .Switch(Switch),  .Mem\_Write(Mem\_Write),  .Clk(Clk),  .LED(LED)  );  initial begin  // Initialize Inputs  Mem\_Addr = 0;  Switch = 0;  Mem\_Write = 0;  Clk = 0;    // Wait 100 ns for global reset to finish  //#100;  // Add stimulus here  #50; Mem\_Addr=6'b000001;Switch=2'b10;Mem\_Write=1;Clk=0;  #50; Mem\_Addr=6'b000001;Switch=2'b10;Mem\_Write=1;Clk=1;  #50; Mem\_Addr=6'b000001;Switch=2'b10;Mem\_Write=0;Clk=0;  #50; Mem\_Addr=6'b000010;Switch=2'b11;Mem\_Write=1;Clk=0;  #50; Mem\_Addr=6'b000010;Switch=2'b11;Mem\_Write=1;Clk=1;  #50; Mem\_Addr=6'b000010;Switch=2'b00;Mem\_Write=0;Clk=0;  #50; Mem\_Addr=6'b000001;Switch=2'b00;Mem\_Write=1;Clk=0;  #50; Mem\_Addr=6'b000001;Switch=2'b00;Mem\_Write=1;Clk=1;  #50; Mem\_Addr=6'b000001;Switch=2'b00;Mem\_Write=0;Clk=0;  #50; Mem\_Addr=6'b000001;Switch=2'b01;Mem\_Write=1;Clk=0;  #50; Mem\_Addr=6'b000001;Switch=2'b01;Mem\_Write=1;Clk=1;  #50; Mem\_Addr=6'b000001;Switch=2'b00;Mem\_Write=0;Clk=0;  end    endmodule | | | | | |
| **二、仿真波形** | | | | | |
| ISim (O.87xd) - [Default.wcfg] | | | | | |
| **三、电路图** | | | | | |
| ISE Project Navigator (O.87xd) - C:\Users\kannaduki\Desktop\ISE\Program5\Program5.xise - [RAM_A (RTL1)] | | | | | |
| **四、引脚配置（约束文件）** | | | | | |
| NET "Mem\_Addr[2]" LOC = T5;  NET "Mem\_Addr[3]" LOC = V8;  NET "Mem\_Addr[4]" LOC = U8;  NET "Mem\_Addr[5]" LOC = N8;  NET "Mem\_Addr[6]" LOC = M8;  NET "Mem\_Addr[7]" LOC = V9;  NET "Switch[0]" LOC = T9;  NET "Switch[1]" LOC = T10;  NET "Mem\_Write" LOC = C4;  NET "Clk" LOC = C9;  NET "LED[0]" LOC = U16;  NET "LED[1]" LOC = V16;  NET "LED[2]" LOC = U15;  NET "LED[3]" LOC = V15;  NET "LED[4]" LOC = M11;  NET "LED[5]" LOC = N11;  NET "LED[6]" LOC = R11;  NET "LED[7]" LOC = T11; | | | | | |
| **五、思考与探索** | | | | | |
|  | | | | | |
| **六、意见和建议** | | | | | |
|  | | | | | |